

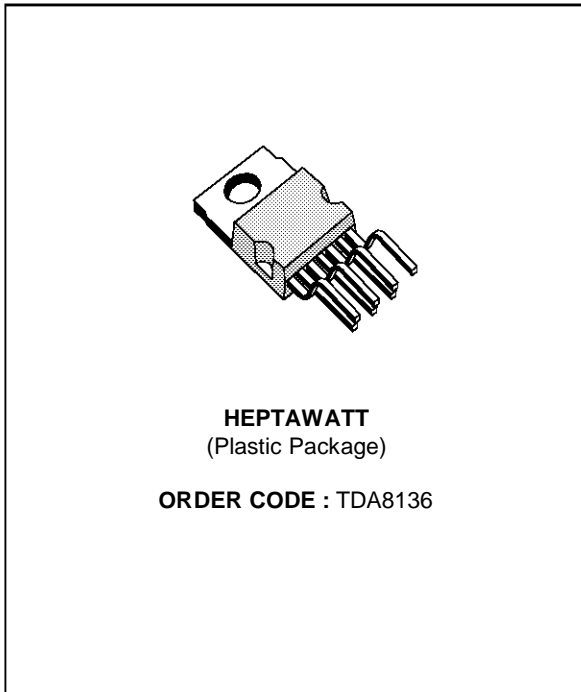
**DUAL 12V REGULATOR WITH DISABLE**

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE  
12V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE  
12V ± 2%
- OUTPUT 2 VOLTAGE DISABLED BY A TTL  
INPUT
- SHORT CIRCUIT PROTECTION AT BOTH  
OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION

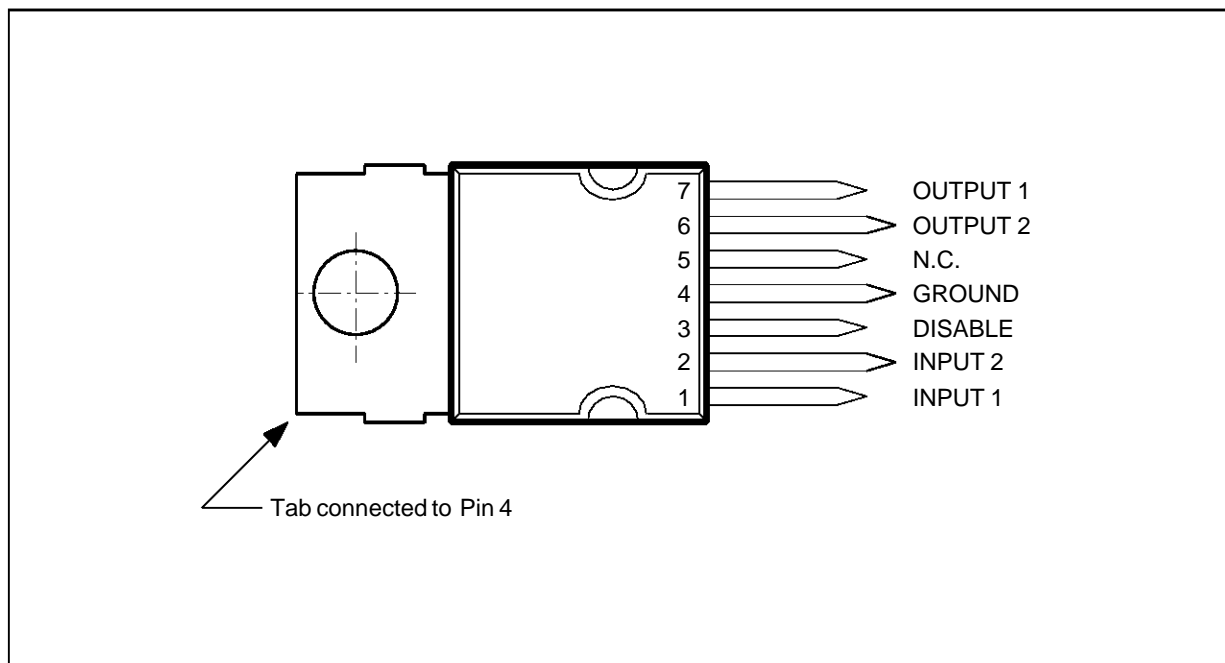
**DESCRIPTION**

The TDA8136 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, both 12V at currents up to 600mA.

Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

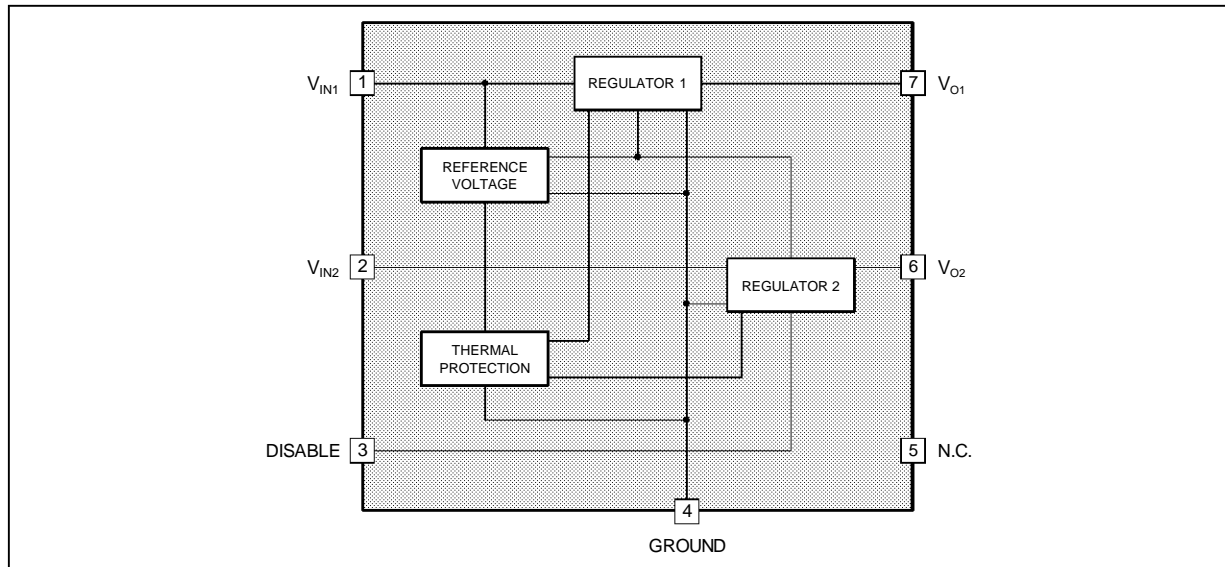


**PIN CONNECTIONS**



8136-01EPS

**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{IN1, 2}$	DC Input Voltages	24	V
$V_{DIS}$	Disable Input Voltage Pin 3	24	V
$I_{O1, 2}$	Output Currents	Internally Limited	
$P_t$	Power Dissipation	Internally Limited	
$T_{STG}$	Storage Temperature	- 65 to + 150	°C
$T_j$	Junction Temperature	0 to + 150	°C

**THERMAL DATA**

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	Max. 3	°C/W

**ELECTRICAL CHARACTERISTICS**

( $V_{IN1,2} = 14V$  ;  $V_{DIS} = 2.5V$  ;  $I_{O1,2} = 0$  ;  $T_j = 25^\circ C$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{O1}$	Output Voltage at Pin 7		11.76	12	12.24	V
$V_{O2}$	Output Voltage at Pin 6		11.76	12	12.24	V
$I_{Q1}$	Quiescent Current	$V_{IN2} = 0, V_{DIS} = 0$ $I_{O1} = 10mA, (see fig. 1)$			2	mA
$I_{Q2}$	Quiescent Current	$I_{O2} = 10mA (see fig. 1)$			2	mA
$V_{IN1}-V_{O1}$	Drop Out Voltage 1	$I_{O1} = 400mA$			1.5	V
$V_{IN2}-V_{O2}$	Drop Out Voltage 2	$I_{O2} = 400mA$			1.5	V
$\Delta V_{O1LI}$	Line Regulation 1	$14V < V_{IN1} < 18V, I_{O1} = 200mA$			120	mV
$\Delta V_{O2LI}$	Line Regulation 2	$14V < V_{IN2} < 18V, I_{O2} = 200mA$			120	mV
$\Delta V_{O1LO}$	Load Regulation 1	$0 < I_{O1} < 600mA$			240	mV
$\Delta V_{O2LO}$	Load Regulation 2	$0 < I_{O2} < 600mA$			240	mV

**ELECTRICAL CHARACTERISTICS** (continued)

( $V_{IN1,2} = 14V$  ;  $V_{DIS} = 2.5V$  ;  $I_{O1,2} = 0$  ;  $T_j = 25^{\circ}C$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{O1SC}$	Short Circuit Current 1	$14V < V_{IN1} < 18V$			1.3	A
$I_{O2SC}$	Short Circuit Current 2	$14V < V_{IN2} < 18V$			1.3	A
$V_{DISH}$	Disable Voltage HIGH at Pin 3		2			V
$V_{DISL}$	Disable Voltage LOW at Pin 3				0.8	V
$I_{DISH}$	Bias Current at Pin 3	$V_{DIS} = 5.3V$			10	$\mu A$
$I_{DISL}$	Bias Current at Pin 3	$V_{DIS} = 0.4V$	-80			$\mu A$
$SVR_1$	Supply Voltage Rejection 1 (see note 1)	$V_{IN1} = 16V_{DC} + 1V_{PP} SIN$ $f = 120Hz, I_{O1} = 200mA$	50			dB
$SVR_2$	Supply Voltage Rejection2 (see note 1)	$V_{IN2} = 16V_{DC} + 1V_{PP} SIN$ $f = 120Hz, I_{O2} = 200mA$	50			dB
$I_Q$	Quiescent Current	$V_{IN1} = V_{IN2} = 14V_{DC}$ $I_{O1} = I_{O2} = 200mA$ (see fig. 1)			6	mA
$T_{JSD}$	Thermal Shut-down Junction Temperature			145		$^{\circ}C$

8136-04.TBL

**Note 1 :** SVR supply voltage rejection :

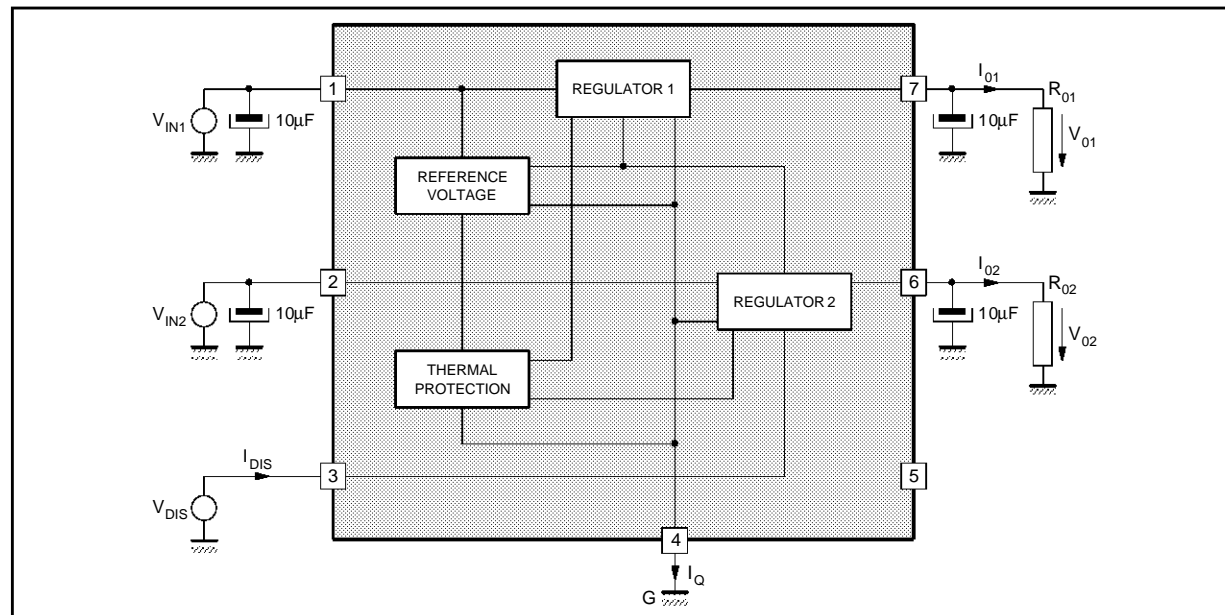
$$20 \cdot \text{LOG} \cdot \left| \frac{V_{INac}}{V_{Oac}} \right|$$

where :

$V_{INac}$  is the value of the sinusoidal signal forced at the input. (120Hz, 1V<sub>PP</sub>)

$V_{Oac}$  is the peak-peak ripple voltage present at the output

**Figure 1 : Test Circuit**



8136-03.EPS

## TDA8136

### CIRCUIT DESCRIPTION

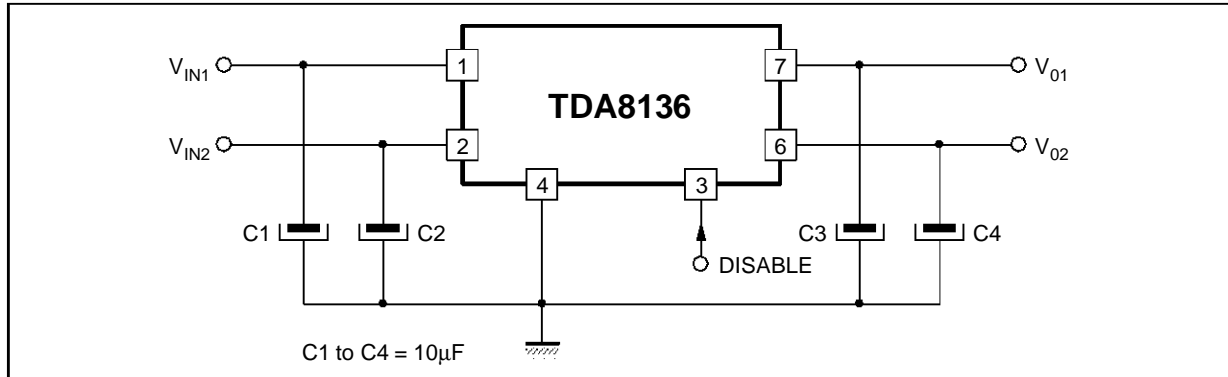
The TDA8136 is a dual voltage regulator with disable.

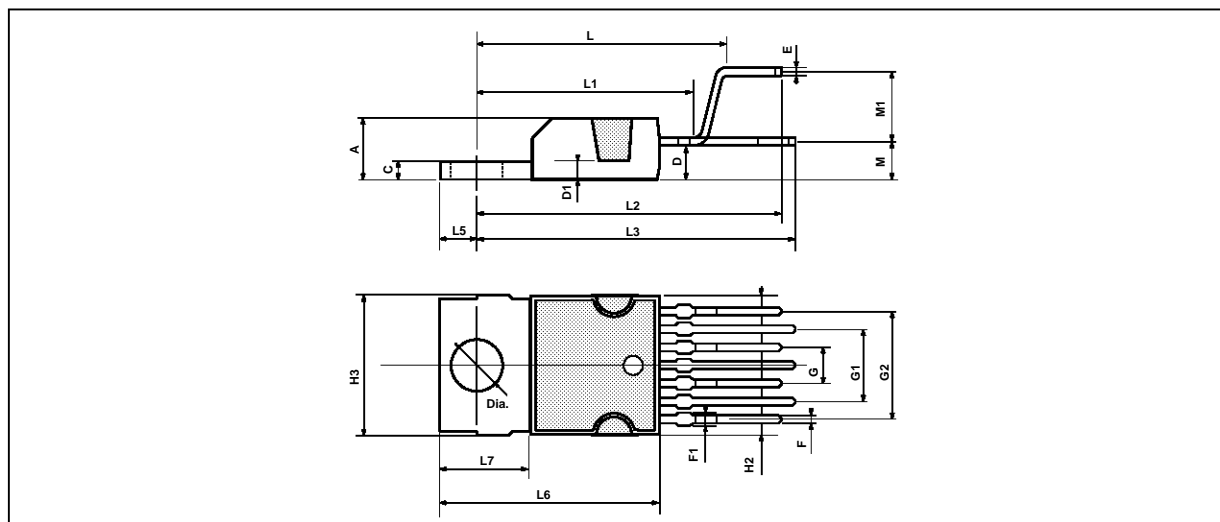
The two regulation parts are supplied from one voltage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this

last is connected at Pin 1 ( $V_{IN1}$ ), the regulator 2 will not work if the Pin 1 is not supplied.

It is possible to switch-off the output voltage 2 ( $V_{O2}$ ) by applying at Pin 3 (disable input) a low TTL level.

### TYPICAL APPLICATION



**PACKAGE MECHANICAL DATA**  
 9 PINS - PLASTIC HEPTAWATT


PM-HEPTV.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia.	3.65		3.85	0.144		0.152

HEPTV.TBL

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